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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/739,226	JOHNSON ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-19 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-19, 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-4, 8, 10-19, 21, and 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Baba et al., Patent No. 5,894,394.

With respect to claim 1, Baba teaches a current monitoring and interrupting circuit [Fig. 10] comprising: an electrically conductive line [Fig. 10; line coming from the power supply terminal 12] carrying a DC current; a sensor [Fig. 10; resistor R1; col. 3 lines 4-5] that outputs a voltage level indicative of a magnitude of the DC current [Fig. 10; the voltage level going into + terminal of the comparator 20]; a comparator [Fig. 10; 20; col. 2 lines 64 – col. 3 lines 3] that compares the voltage level to a reference potential [Fig. 10; Vref; col. 3 lines 4-10] and generates a circuit indicator signal [Fig. 10; a signal coming out from the comparator 20 and going into a logical summation circuit 23]; and a logic-based current interrupter [Fig. 10; 17; col. 2 lines 46-54] that generates a second signal [Fig. 10; a signal coming out from Q to transistor 18] in response to the circuit indicator signal; a current switch [Fig. 10; 15] that selectively prevents the flow of current in the electrically conductive line [Fig. 10; line coming from the power supply terminal 12] in response to the second signal [col. 2 line 64 - col. 3 lines 27].

With respect to claim 3, Baba teaches that the current switch [Fig. 10; 15] includes a MOSFET [col. 2 lines 35-45].

With respect to claim 4, Baba further includes a fuse [Fig. 9; fuse FL9] disposed in the electrically conductive line [col. 2 lines 17-23].

With respect to claim 8, Baba teaches that the electrically conductive line is part of a vehicular electrical bus [col. 1 lines 5-15].

With respect to claim 10, Baba teaches that the logic-based current interrupter [Fig. 10; 17] includes a Boolean logic device [col. 2 lines 46-54].

With respect to claim 11, Baba teaches that Boolean logic device includes a flip flop [Fig. 10; flip-flop 17; col. 2 line 50].

With respect to claim 12, Baba further includes a reset circuit [Fig. 10, consists of resistor R1, comparator 20, and logic circuit 23].

With respect to claim 13, Baba further includes an indicator that signals [Fig. 10; the signal coming out of the comparator 20] whether the current is flowing in the electrically conductive line.

With respect to claim 14, Baba teaches a method [Fig. 10] of monitoring and interrupting DC current flowing in an electrically conductive line [Fig. 10; line coming from the power supply terminal 12], comprising sensing [Fig. 10; resistor R1; col. 3 lines 4-5] the DC current flowing in the electrically conductive line; generating a voltage level

indicative of a magnitude of the DC current [Fig. 10; the voltage level going into + terminal of the comparator 20]; comparing the voltage level to a reference voltage [Fig. 10; Vref; col. 3 lines 4-10] and generating a circuit indicator signal [Fig. 10; a signal coming out from the comparator 20 and going into a logical summation circuit 23]; and using a logic-based device [Fig. 10; 17; col. 2 lines 46-54] to prevent the flow of the DC current flowing in the electrically conductive line if the circuit indicator signal is indicative of a condition where the voltage level is higher than the reference voltage [col. 2 line 64 - col. 3 lines 27].

With respect to claim 15, Baba teaches that the logic-based device [Fig. 10; 17] includes a flip flop [Fig. 10, flip-flop 17] that controls a current switch [Fig. 10, 15].

With respect to claim 16, Baba teaches that the current switch [Fig. 10; 15] includes a MOSFET [col. 2 lines 35-45].

With respect to claim 17, Baba further includes resetting the logic-based device [Fig. 10; flip-flop 17] to restore the current flowing in the electrically conductive line [Fig. 10; resetting circuit is made up of resistor R1, comparator 20, and logic circuit 23].

With respect to claim 18, Baba teaches that the step of resetting is performed automatically [Fig. 10; the resetting circuit, which is made up of resistor R1, comparator 20, and logic circuit 23, reset the flip flop automatically].

With respect to claim 19, Baba further includes generating an indicator signal [Fig. 10; the output of the comparator 20] that conveys whether the current is flowing in the electrically conductive line.

With respect to claim 21, Baba teaches a circuit breaker [Fig. 10; switching circuit 11] for interrupting a flow of DC current in an electrically conductive line [Fig. 10; line coming from the power supply terminal 12] comprising a sensor [Fig. 10; resistor R1; col. 3 lines 4-5] that outputs a voltage level indicative of a magnitude of the DC current [Fig. 10; the voltage level going into + terminal of the comparator 20]; a comparator [Fig. 10; comparator 20] that compares the voltage level to a reference potential [Fig. 10; Vref; col. 3 lines 4-10] and generates a circuit indicator signal [Fig. 10; a signal coming out from the comparator 20 and going into a logical summation circuit 23]; a logic device [Fig. 10; 17; col. 2 lines 46-54] that receives the circuit indicator signal and generates a current interrupt signal [Fig. 10; a signal coming out from Q to transistor 18] when the circuit indicator signal corresponds to a condition where the voltage level is greater than the reference potential [col. 2 lines 64 – col. 3 lines 3]; and a current switch [Fig. 10; 15] that selectively prevents the flow of current in the electrically conductive line in response to the current interrupt signal [col. 2 line 64 - col. 3 lines 27].

With respect to claim 23, Baba teaches that the logic device [Fig. 10; 17] includes a flip flop [Fig. 10, flip-flop 17].

With respect to claim 24, Baba teaches that the current switch [Fig. 10; 15] includes a MOSFET [col. 2 lines 35-45].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-7, 9, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba et al., Patent No. 5,894,394, in view of Huang et al., Patent No. 6,952,335.

Baba discloses an electrically conductive line, but does not disclose that the electrically conductive line is part of an electrical bus energized to at least 60 VDC, 200 VDC, or 300 VDC. Huang teaches a solid-state DC circuit breaker.

With respects to claims 5-7, Huang teaches that the electrically conductive line is part of an electrical bus energized to at least 60, 200 and 300 VDC. [Abstract, liens 1-2, Col. 3, lines 56-57, The DC circuit breaker is capable of interrupting high DC currents, which means the circuit breaker is connected across a high voltage source, which can include 60 VDC, 200 VDC, and 300 VDC].

Baba and Huang are analogous monitoring and interrupting circuits connected between power supply and loads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Huang, which teaches high voltage sources, with the circuit of Baba, for the benefit of providing a circuit breaker that is capable of interrupting high DC currents, which come from high DC voltages.

With respect to claim 9, Huang teaches that the sensor includes a Hall Effect device [Col. 4, lines 62-67].

With respect to claim 22, Huang teaches that the sensor includes a Hall Effect current transducer [Col. 4, lines 62-67].

Response to Arguments

Applicant's arguments with respect to claims 1, 3-19, 21-24 have been considered but are moot in view of the new ground(s) of rejection.

Applicant comments in the REMARKS that the prior art does not disclose a current switch that selectively prevents the flow of current in the electrically conductive line.

The Examiner points out that a new reference by Baba et al. [Patent No. 5,894,394] has been introduced to meet this limitation.

Based on examiner's best understanding, it is believed that the prior art reference by Baba et al. reads on the amended claim language of independent claims 1, 14, and 21.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 7:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2800, Ext. 36. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dharti H. Patel/
GAU 2836
11/12/2007

11/13/07

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